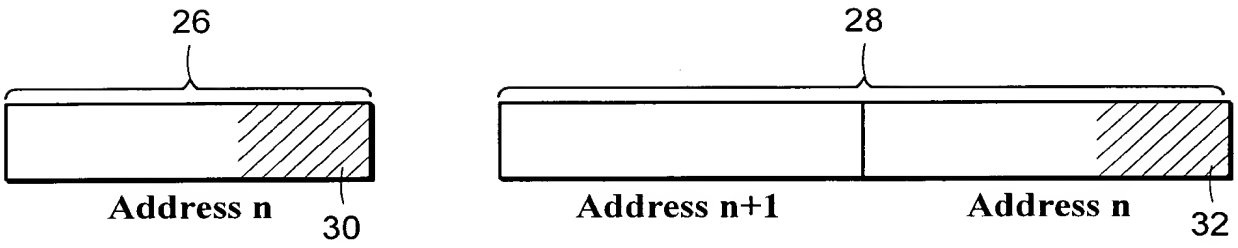

FIG. 1
(PRIOR ART)

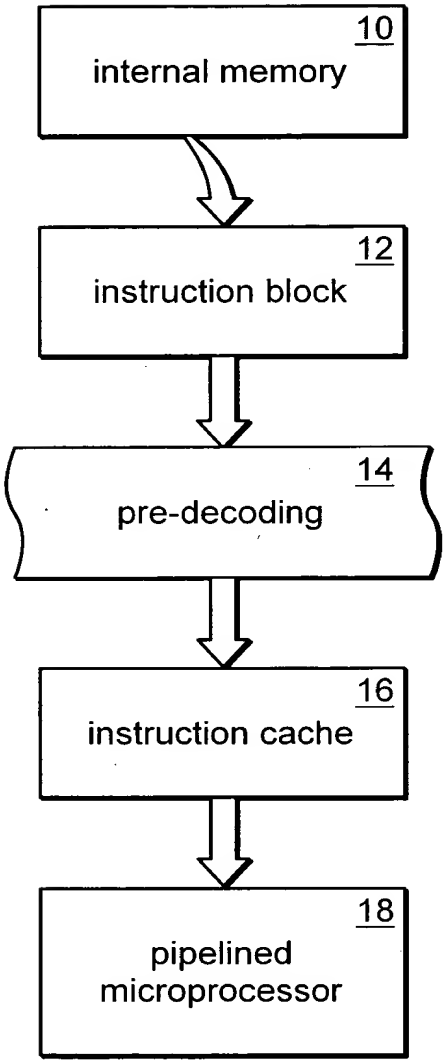

FIG. 2
(PRIOR ART)

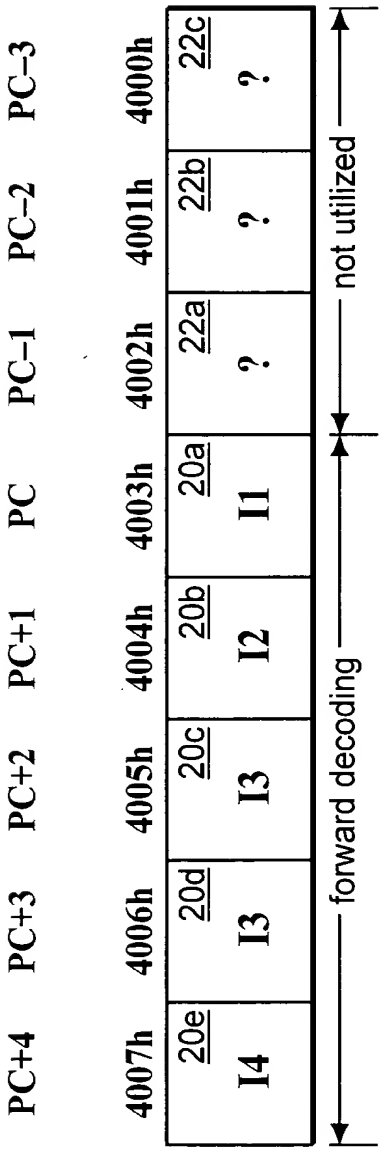

FIG. 3
(PRIOR ART)

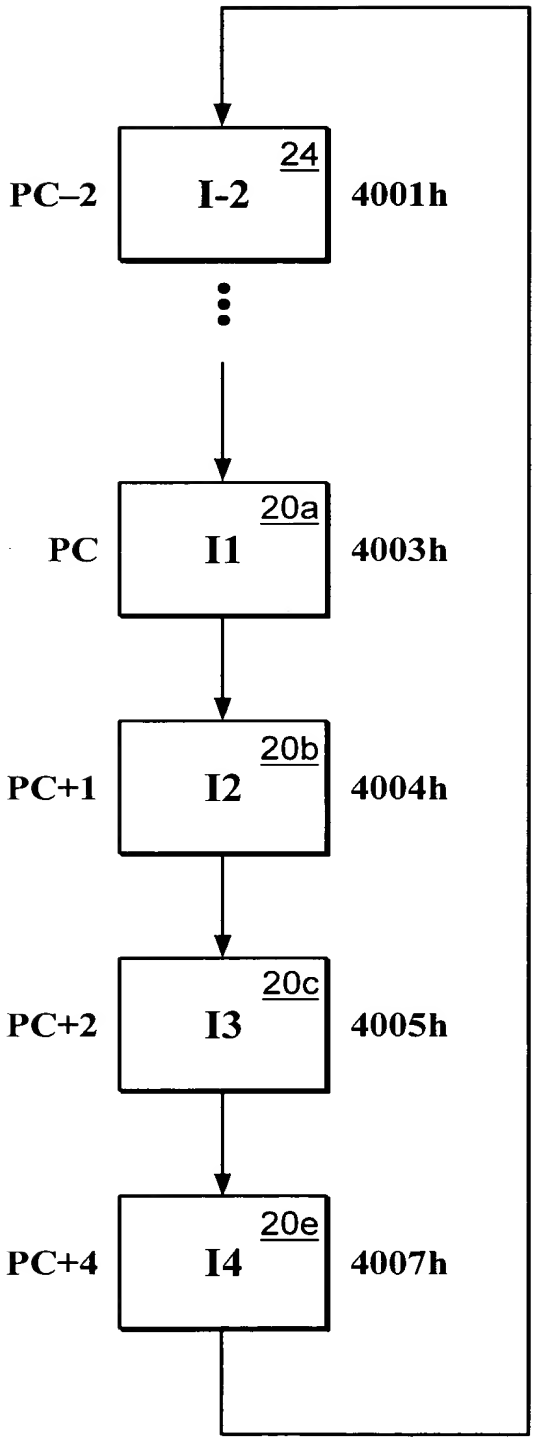

FIG. 4
(PRIOR ART)

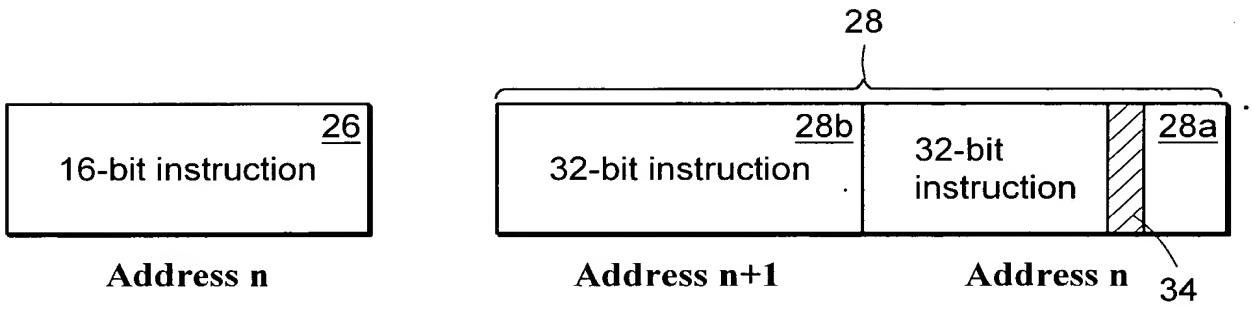
28
26
16-bit instruction
28b
32-bit instruction
32-bit instruction
28a
Address n
Address n+1
Address n
34

FIG. 5

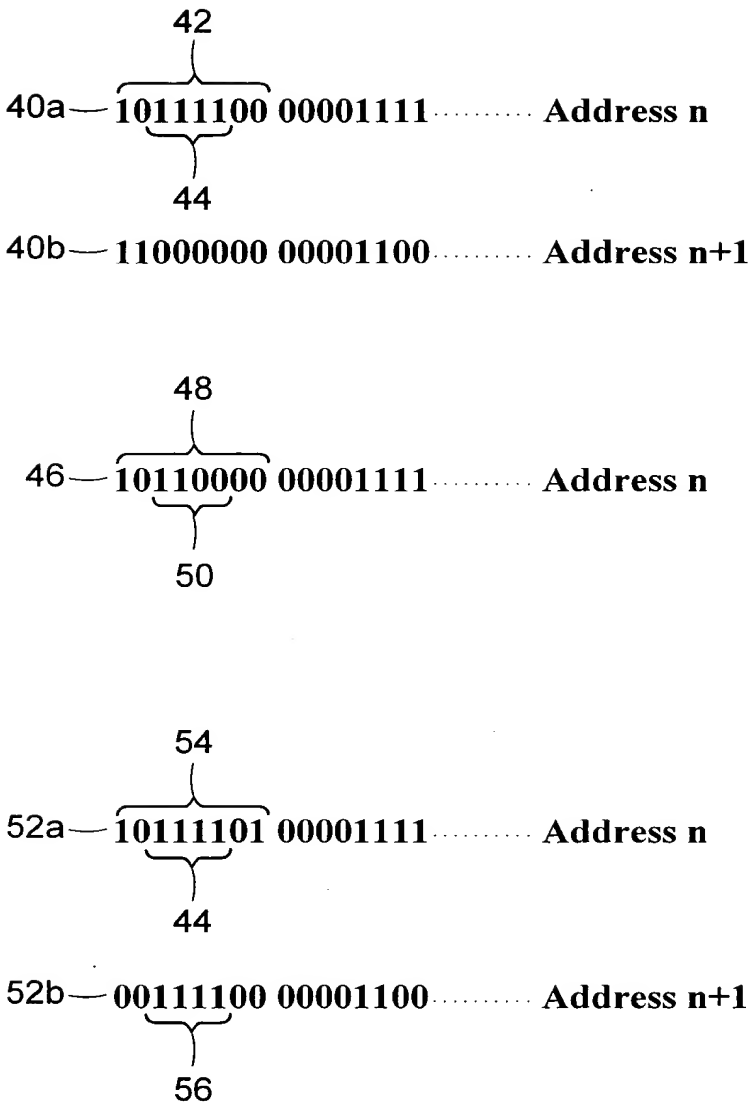
42
40a
10111100 00001111
Address n
44
40b
11000000 00001100
Address n+1
48
46
10110000 00001111
Address n
50
54
52a
10111101 00001111
Address n
44
52b
00111100 00001100
Address n+1
56

FIG. 6

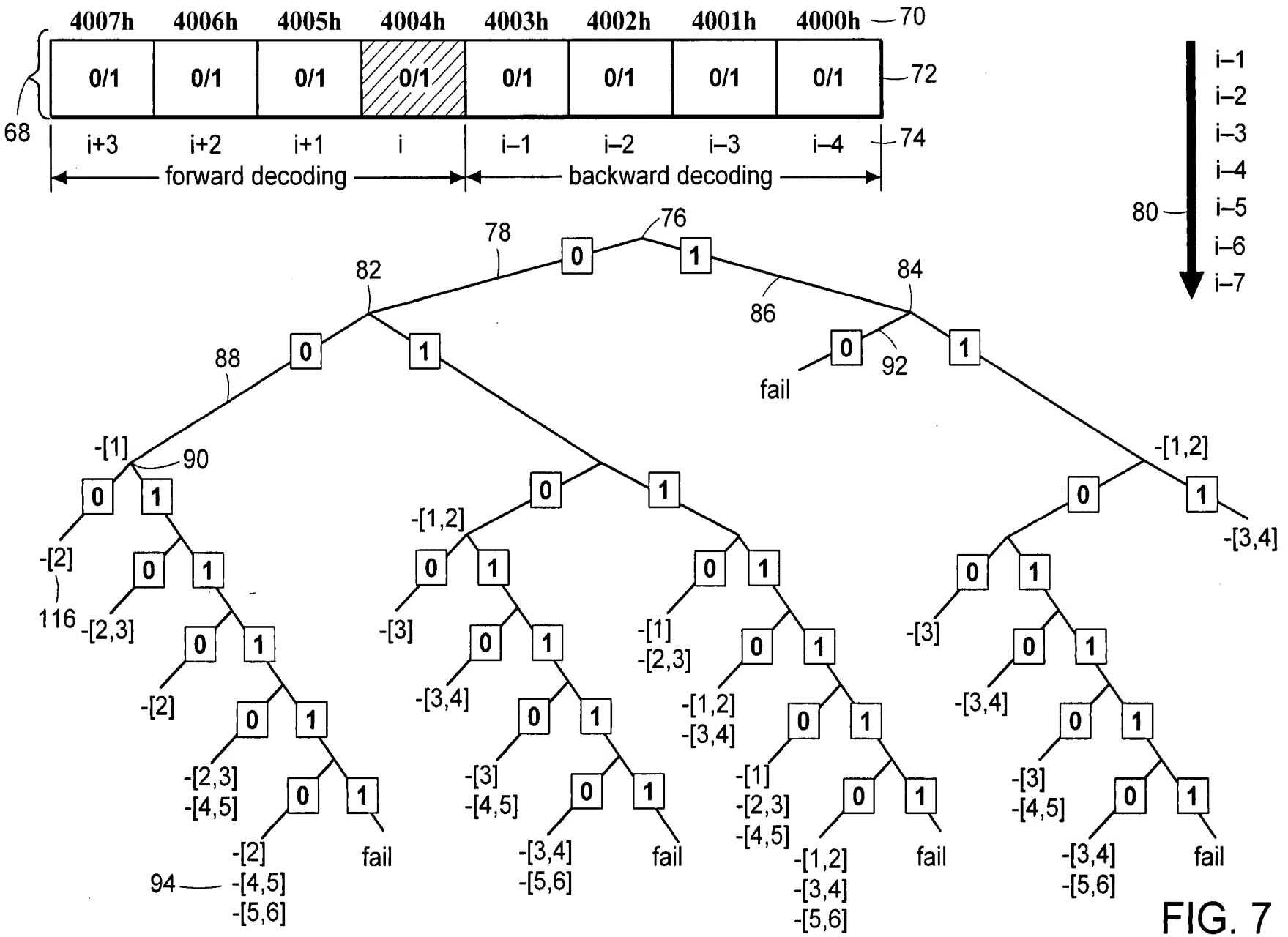
4007h
4006h
4005h
4004h
4003h
4002h
4001h
4000h
70
0/1
0/1
0/1
0/1
0/1
0/1
0/1
0/1
72
68
i+3
i+2
i+1
i
i–1
i–2
i–3
i–4
74
forward decoding
backward decoding
80
i–1
i–2
i–3
i–4
i–5
i–6
i–7
78
76
82
84
86
88
fail
92
-[1]
90
-[1,2]
-[2]
116
-[2,3]
-[3]
-[3,4]
-[1]
-[2,3]
-[1,2]
-[3,4]
-[2,3]
-[4,5]
-[3]
-[4,5]
-[1]
-[2,3]
-[4,5]
-[3]
-[4,5]
-[2]
94
-[4,5]
-[5,6]
fail
-[3,4]
-[5,6]
fail
-[1,2]
-[3,4]
-[5,6]
fail
-[3,4]
-[5,6]
fail

FIG. 7

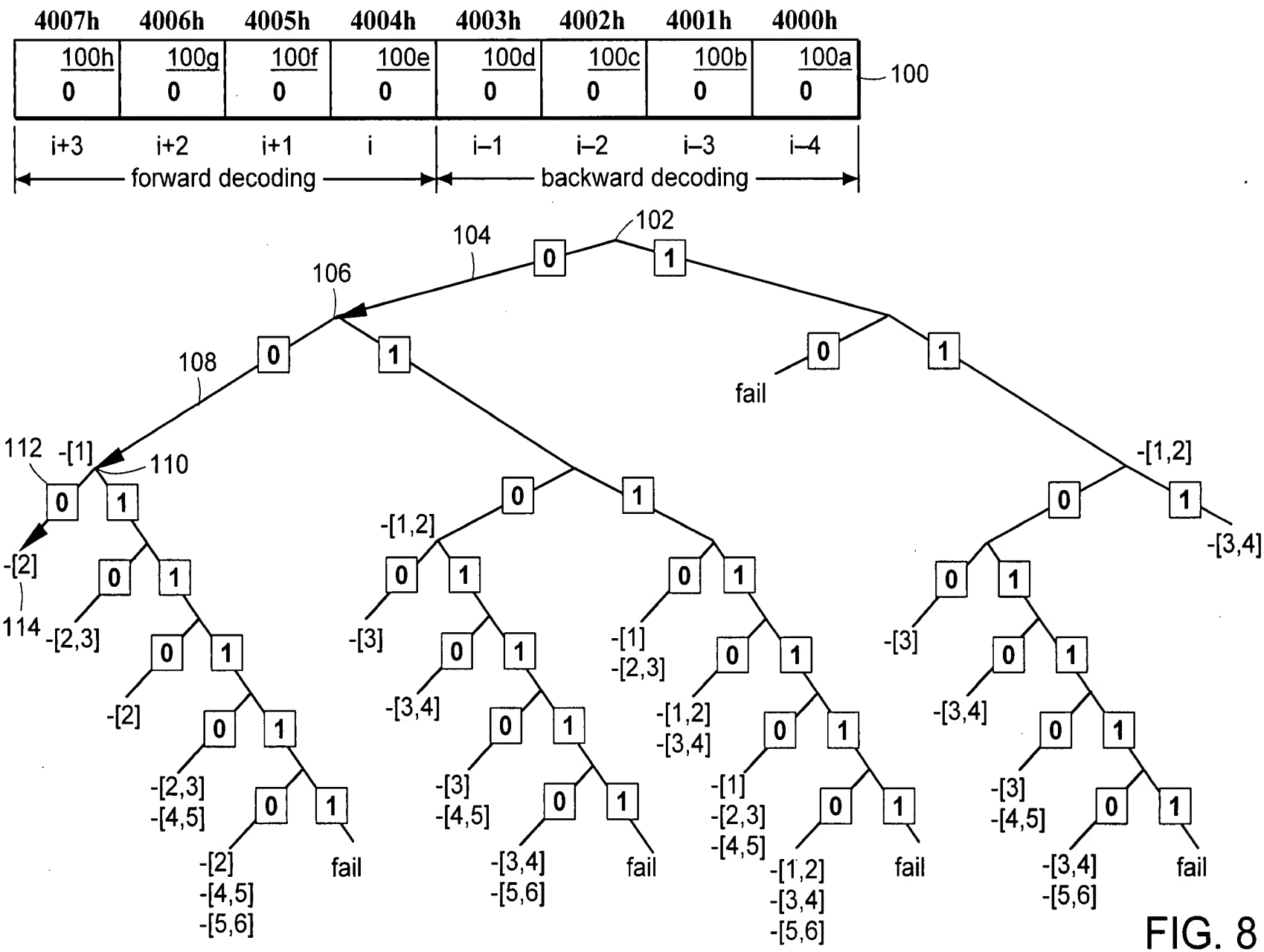
4007h
4006h
4005h
4004h
4003h
4002h
4001h
4000h
100h
100g
100f
100e
100d
100c
100b
100a
0
100
i+3
i+2
i+1
i
i–1
i–2
i–3
i–4
forward decoding
backward decoding
104
102
106
108
112
-[1]
110
fail
-[1,2]
-[2]
114
-[2,3]
-[3]
-[3,4]
-[1]
-[2,3]
-[1,2]
-[3,4]
-[2,3]
-[4,5]
-[3]
-[4,5]
-[1]
-[2,3]
-[4,5]
-[2]
-[4,5]
-[5,6]
-[3,4]
-[5,6]
-[1,2]
-[3,4]
-[5,6]
-[3]
-[4,5]
-[3,4]
-[5,6]
fail

FIG. 8

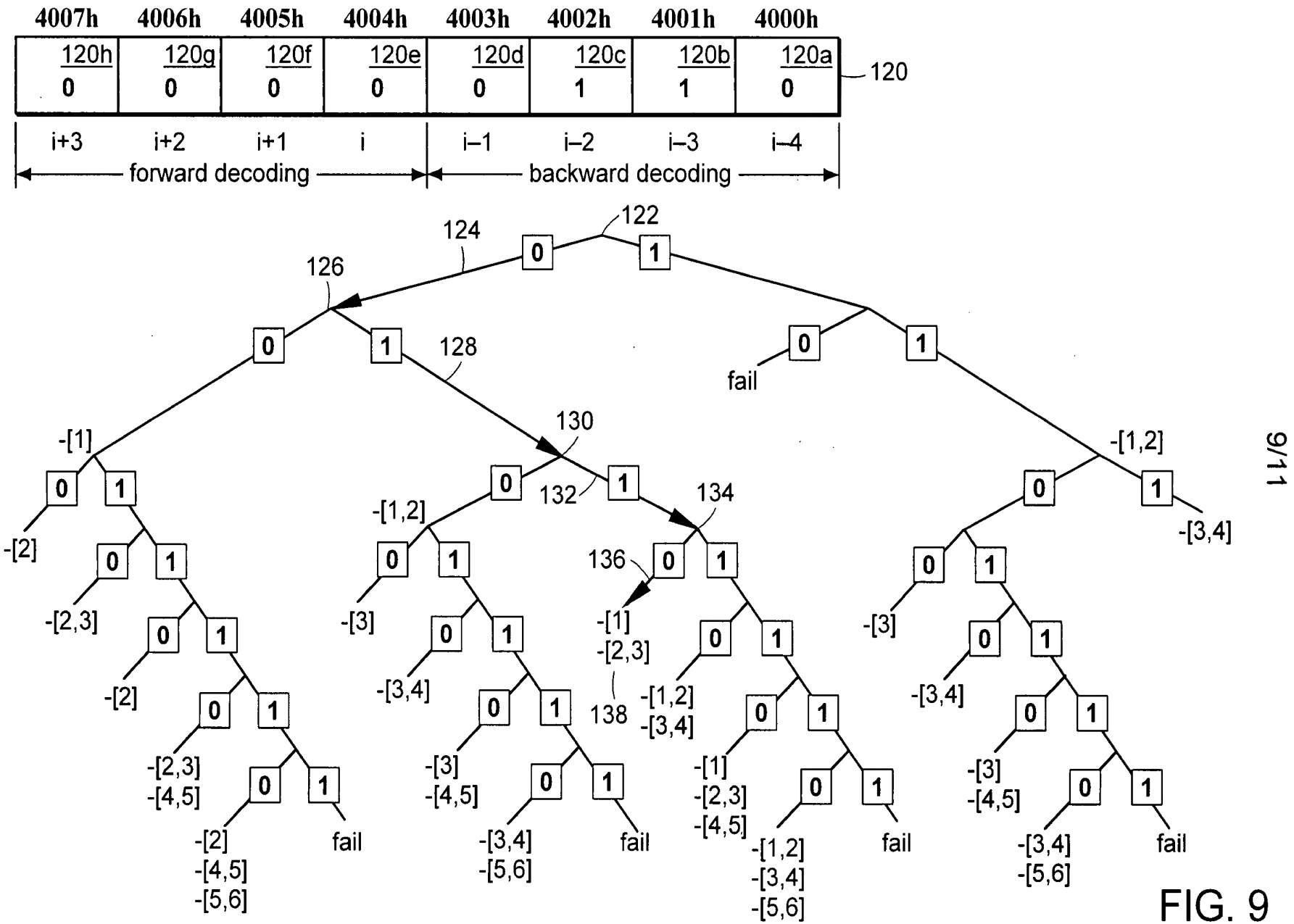
4007h
4006h
4005h
4004h
4003h
4002h
4001h
4000h
120h
120g
120f
120e
120d
120c
120b
120a
0
0
0
0
0
1
1
0
120
i+3
i+2
i+1
i
i–1
i–2
i–3
i–4
forward decoding
backward decoding
122
124
126
128
130
132
134
136
138
fail
-[1]
-[2]
-[2,3]
-[2]
-[2,3]
-[4,5]
-[2]
-[4,5]
-[5,6]
fail
-[1,2]
-[3]
-[3,4]
-[3]
-[4,5]
-[3,4]
-[5,6]
fail
-[1]
-[2,3]
-[1,2]
-[3,4]
-[1]
-[2,3]
-[4,5]
-[1,2]
-[3,4]
-[5,6]
fail
-[1,2]
-[3,4]
-[3]
-[3,4]
-[3]
-[4,5]
-[3,4]
-[5,6]
fail

FIG. 9

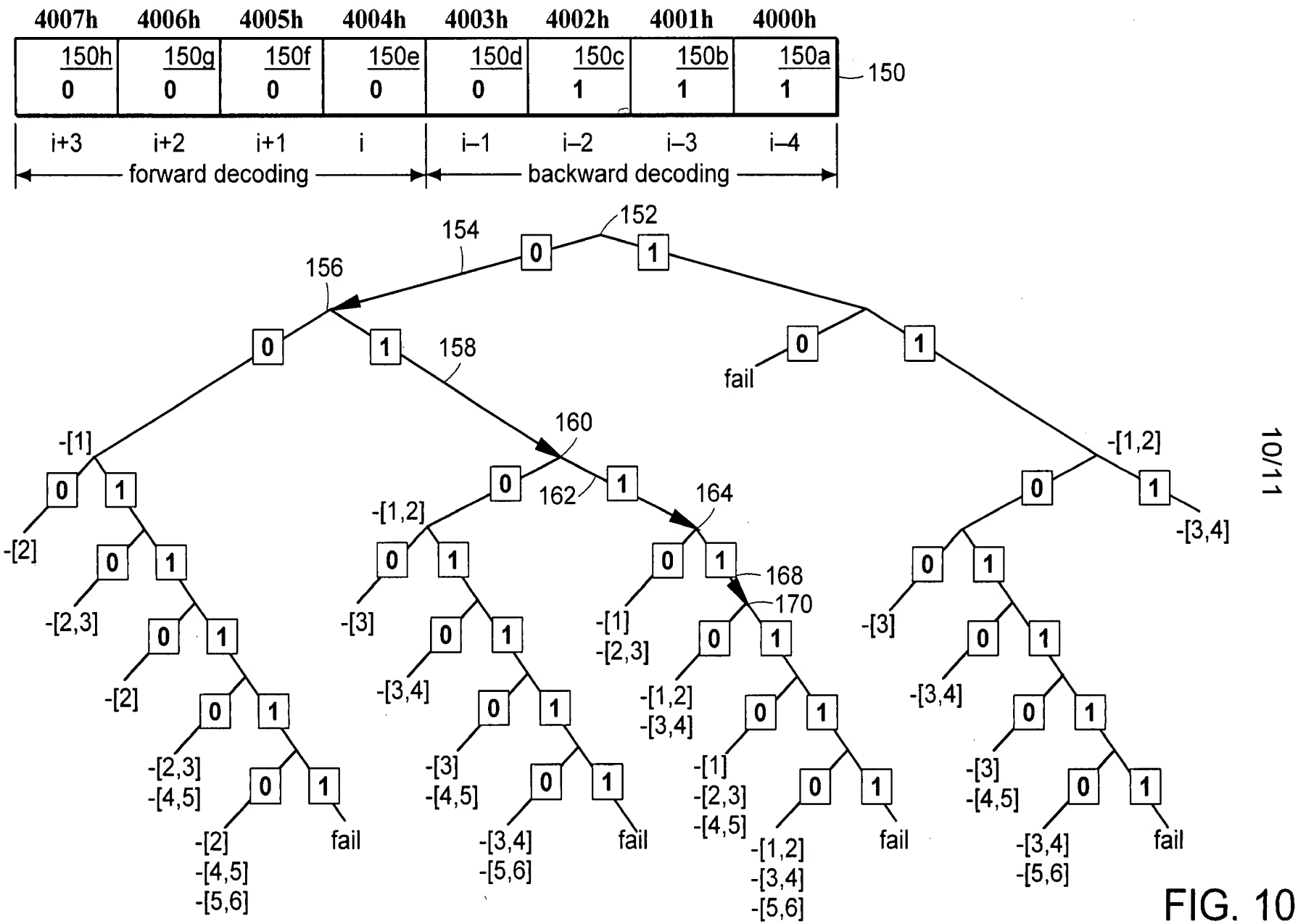
4007h
4006h
4005h
4004h
4003h
4002h
4001h
4000h
150h
150g
150f
150e
150d
150c
150b
150a
0
0
0
0
0
1
1
1
150
i+3
i+2
i+1
i
i–1
i–2
i–3
i–4
forward decoding
backward decoding
152
154
156
158
160
162
164
168
170
fail
-[1]
-[2]
-[2,3]
-[2]
-[2,3]
-[4,5]
-[2]
-[4,5]
-[5,6]
fail
-[1,2]
-[3]
-[3,4]
-[3]
-[4,5]
-[3,4]
-[5,6]
fail
-[1]
-[2,3]
-[1,2]
-[3,4]
-[1]
-[2,3]
-[4,5]
-[1,2]
-[3,4]
-[5,6]
fail
-[1,2]
-[3,4]
-[3]
-[3,4]
-[3]
-[4,5]
-[3,4]
-[5,6]
fail

FIG. 10

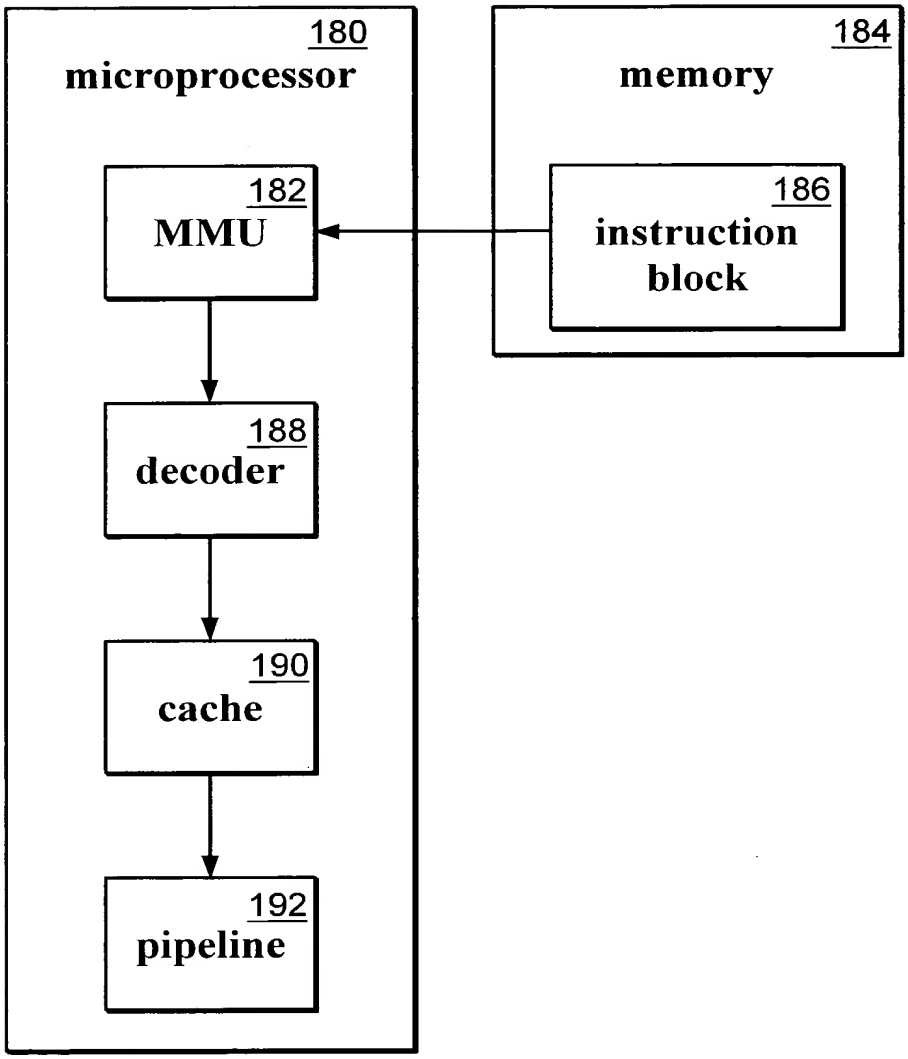
180
microprocessor
182
MMU
188
decoder
190
cache
192
pipeline
184
memory
186
instruction block

FIG. 11